App. Serial No.: 10/801,942
Atty. Docket No.: 0057-011

## REMARKS

These remarks are in response to the Office Action dated June 19, 2008, which has a shortened statutory period for response set to expire September 19, 2008. A three-month extension, to expire December 19, 2008, is requested in a petition filed herewith.

Claims

Claims 1-26, 29-38, and 40-59 are pending in the above-identified application. Claims 1-26, 29-38, and 40-59 are rejected over prior art. Claims 1, 14-16, 19, 23, 30, 36, 42-43, 50, 53, and 56-59 are amended and Claims 27-28, 31-33, and 37-39 are canceled. Claims 2, 5-6, 9-10, 18, 20-22, and 25-26 remain as filed, and Claims 3-4, 7-8, 11-13, 17, 24, 29, 34-35, 40-41, 44-49, 51-52, and 54-55 remain as previously presented. Reconsideration is requested.

Claim Objections

Claim 43 is objected to because it contains two consecutive "ands." Claim 43 is amended herein to remove one of the "ands." Therefore, Applicant respectfully requests withdrawal of the objection to Claim 43.

Rejections Under 35 U.S.C. § 112

The heading "Claim Rejections - 35 USC § 112" appears at page 2, paragraph 5 of the Office Action followed by a quotation of 35 U.S.C. § 112, second paragraph. However, no detailed rejections of any claim appears after the heading. Therefore, it appears to Applicant that there are no outstanding rejections under 35 U.S.C. § 112, second paragraph.

Rejections Under 35 U.S.C. § 102

Claims 50-55, 58, and 59 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent App. Pub. No. 2004/0107332 (Fujii et al.).

Claims 50-52:

With respect to Claim 50, the Examiner writes:

> Regarding claim 50, Fujii discloses a computer array, comprising: a plurality of computers each hard wired to communicate with at least three of the plurality of computers (fig.

> 11); and a plurality of data paths connecting the computers, each of the data paths being dedicated to an adjacent pair of the computers ([0072]); and wherein, at least some of the computers are assigned a task different from that assigned to the other computers ([0008]).

Applicant respectfully requests reconsideration.

The standard for anticipation is set forth in M.P.E.P. § 2131 as follows:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

As previously presented, Claim 50 recited (in part) "a plurality of computers each hard wired to communicate with at least three of the plurality of computers." Fujii et al. does not disclose this limitation of Claim 50.

Initially, Applicant would like to point out that it is somewhat unclear what the Examiner is characterizing as "a plurality of computers" in Fujii et al. For example, paragraph [0072] discusses both processor elements 102 and state control units 101, paragraph [0008] discusses a plurality of processor elements (such as processor elements 102), and FIG. 11 shows only state control units 101 and event communication lines 145. Accordingly, it appears to Applicant that the Examiner is characterizing either the processor elements 102 or the state control units 101 in Fujii et al. as an equivalent to the term "computer" in Claim 50. Therefore, Applicant will address each possible characterization in turn.

In summary, an embodiment of Applicant's invention provides a plurality of independent computers, all integrated on a single chip. Each of the computers includes (among other elements) its own processor, its own random-access memory (RAM), and its own read-only memory (ROM). Each computer can be programmed to accomplish any desired task and can operate independently of and/or in cooperation with the other computers. In a particular embodiment of the invention, the computers are identical, general purpose computers. In another particular embodiment, a computer can be programmed to service an input/output port for the chip or can be programmed to service off-chip RAM or flash memory. Of course, that computer

could also be programmed to perform additional different tasks, such as passing data from one computer to another.

In contrast, Fujii et al. discloses a single array-type processor 100 that includes a plurality of processor elements 102 that are controlled by a plurality of state control units 101 (*Fujii et al.*, paragraph [0042] ). Each of the state control units 101 is connected to the processor elements 102 in an associated element area 105 ( [0043] ). The state control units 101 control the state transitions of the processor elements 102 causing processor elements 102 to process data ( [0048] ).

The processor elements 102 in Fujii et al. cannot be considered "computers" as recited in Claim 50. As described above, processor elements 102 are not independently functioning, but operate under the control of the state control units 101. In addition, each of the processor elements 102 in Fujii et al. do not appear to include dedicated RAM and ROM.

Fujii et al. also does not disclose "a plurality of data paths connecting the computers, each of the data paths being dedicated to an adjacent pair of the computers," as recited by Claim 50. Rather, Fujii et al. discloses that switching elements 108 control the connection relationship between different processor elements 102 via data busses 109 and 110 ( [0009], [0049], [0061], and [0062]; FIGs. 3-5). Accordingly, mb-busses 109 and nb-busses 110 are not "dedicated to an adjacent pair of the computers" as recited by Claim 50.

Like processor elements 102, state control units 101 are also not independently functioning computers. As described above, state control units 101 control the state transitions of processor elements 102 that cause the processor elements 102 to process data ([0015], [0048], [0055], [0078]-[0080]). Accordingly, state control units 101 assign tasks to processor elements 102 to be executed rather than execute those tasks themselves. In addition, it does not appear that state control units 101 include a processing unit, RAM, or ROM.

For the above reasons, Fujii et al. does not disclose "a plurality of computers each hard wired to communicate with at least three of the plurality of computers," or "a plurality of data paths connecting the computers, each of the data paths being dedicated to an adjacent pair of the computers" as recited by Claim 50. However, Applicant is aware that Claim 50 may not have distinguished the invention as clearly as it could have over mere processor arrays. Therefore, Claim 50 is amended herein to more clearly set forth the differences between Applicant's invention and the prior art. In particular, amended Claim 50 now recites (in part) that "each of

the plurality of computers includes read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions." Applicant's original specification provides support for the amendments made to Claim 50 at least at page 6, line 29 to page 7, line 2 and page 4, lines 17-18.

For the above reasons, because the cited prior art does not disclose all the limitations of amended Claim 50, the cited prior art does not anticipate amended Claim 50. Claims 51-52 depend directly from Claim 50 and are, therefore, distinguished from the cited prior art for at least the same reasons as Claim 50.

Claims 53-55:

Similar to Claim 50, Claim 53 is amended herein to recite (in part) that "each of the plurality of computers includes read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions." For the same reasons provided above with respect to Claim 50, Fujii et al. does not disclose all the limitations of amended Claim 53. Because Fujii et al. does not disclose all the limitations of amended Claim 53, Fujii et al. does not anticipate amended Claim 53. Claims 54-55 depend directly from Claim 53 and are, therefore, distinguished from the cited prior art for at least the same reasons as Claim 50.

Claims 58-59:

Like Claim 50, each of Claims 58 and 59 is amended to recite (in part) that "each of the plurality of computers includes read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions." For the same reasons provided above with respect to Claim 50, Fujii et al. does not disclose all the limitations of either of amended Claims 58 or 59. Because Fujii et al. does not disclose all the limitations of amended Claims 58 or 59, Fujii et al. does not anticipate either of amended Claims 58 or 59.

For the above reasons Applicant requests reconsideration and withdrawal of the rejections under 35 U.S.C. § 102.

Rejections Under 35 U.S.C. § 103

Claims 1-4, 6-14, 17-21, 23-26, 30, 32, 34, 41-42, 45-49, and 57 are rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Pat. App. Pub. No. 2004/0107332 (Fujii et al.) in view of U.S. Patent No. 6,023, 753 (Pechanek et al., hereinafter "Pechanek1").

Applicant respectfully requests reconsideration.

Claims 1-4, 6-13, 30, 32, 34, 41, and 45-49:

Regarding Claim 1, the Examiner writes (in part):

> Regarding claim 1, Fujii discloses a computer array, comprising: ...
> Fujii fails to disclose that the computers are integrated on a unitary substrate.
> Pechanek1 discloses a plurality of computers on an array on an integrated circuit (col 2 lines 24-27).
> ....

Applicant respectfully requests reconsideration.

As previously presented, Claim 1 recited "a plurality of computers integrated on a unitary substrate." For the reasons provided above with respect to Claim 50, Fujii et al. does not teach or suggest this element of Claim 1. Similarly, Pechanek1 also does not teach or suggest this element of Claim 1.

Like Fujii et al., Pechanek1 does not teach or suggest an array of independently functioning computers integrated on a unitary substrate. Rather, Pechanek1 discloses a single computer with an array of processing elements (*Pechanek1*, FIGs. 1, col. 1, lines 42-46). For example, the processing elements in Pechanek1 can be separate micro-processor chips (col. 2, lines 25-29). Pechanek1 also states that the "processing element clusters are, as the name implies, groups of processors formed preferably in close physical proximity to one another" (col. 4, lines 7-9).

As discussed above, Applicant is aware that previously presented Claim 1 may not have distinguished the invention clearly over mere processor arrays. Therefore, Claim 1 is amended herein to recite (in part) that each of the plurality of computers includes "read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions."

For the above reasons, because the cited prior art does not teach or suggest all the limitations of amended Claim 1, no prima facie case of obviousness is established with respect to Claim 1. Claims 2-4, 6-13, 30, 32, 34, 41, and 45-49 depend, either directly or indirectly, from Claim 1 and are distinguished, therefore, from the cited prior art for at least the same reasons provided above with respect to Claim 1.

Claims 14 and 17-18:

Claim 14 is amended herein to recite (in part) that each of the plurality of computers includes "read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions." Therefore, Claim 14 is distinguished over the cited prior art for at least the reasons provided above with respect to Claim 1. Claims 17-18 depend from Claim 14 and are distinguished, therefore, from the cited prior art for at least the same reasons as Claim 14.

Claims 19-21:

Claim 19 is amended herein to recite (in part) that each of the plurality of computers includes "read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions." Therefore, Claim 19 is distinguished over the cited prior art for at least the reasons provided above with respect to Claim 1. Claims 20-21 depend from Claim 19 and are distinguished, therefore, from the cited prior art for at least the same reasons as Claim 19.

Claims 23-26:

Claim 23 is amended herein to recite (in part) that each of the plurality of computers includes "read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions." Therefore, Claim 23 is distinguished over the cited prior art for at least the reasons provided above with respect to Claim 1. Claims 24-26 depend from Claim 23 and are distinguished, therefore, from the cited prior art for at least the same reasons as Claim 23.

Claim 42:

Claim 42 is amended herein to recite (in part) that each of the plurality of computers includes "read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions." Therefore, Claim 42 is distinguished over the cited prior art for at least the reasons provided above with respect to Claim 1.

Claim 57:

Claim 57 is amended herein to recite (in part) that each of the plurality of computers includes "read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions." Therefore, Claim 57 is distinguished over the cited prior art for at least the reasons provided above with respect to Claim 1.

Claims 5, 22, 29, 35, 36, 43, 44, and 56

Claims 5, 22, 29, 35, 36, 43, 44, and 56 are rejected under 35 U.S.C. §103(a) as being unpatentable over Fujii et al. and Pechanek1 in view of Common Art.

Applicants respectfully request reconsideration.

Claim 43 is amended herein to recite (in part) that "each of the plurality of computers includes read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions." Similarly, Claim 56 is also amended herein to recite (in part) that "each of the computers includes dedicated read-only memory for storing data and instructions, dedicated random access memory for storing data and instructions, and a processor for executing the instructions." Claim 22 depends from Claim 19, Claims 5, 29, 35, and 36 depend, either directly or indirectly, from Claim 1, and Claim 44 depends from Claim 43. Therefore, for the same reasons provided above with respect to Claim 1, because the combination of Fujii et al. and Pechanek1 fails to disclose all of the elements of the claims, the rejections of Claims 5, 22, 29, 35, 36, 43, 44, and 56 under 35 U.S.C. §103 are improper. Reconsideration and withdrawal of the rejections of Claims 5, 22, 29, 35, 36, 43, 44, and 56 is, therefore, respectfully requested.

Furthermore, Applicant strongly objects to the Examiner taking official notice that asynchronous communication between computers (Claims 5, 22, 35, 44, and 56) and asynchronous operation of the computers (Claims 29, 35, 43, and 56) are common in the art. M.P.E.P. § 2144.03(A) sets forth when the examiner may take official notice and provides the following:

> Official notice without documentary evidence to support an examiner's conclusion is permissible only in some circumstances. While "official notice" may be relied on, these circumstances should be rare when an application is under final rejection or action under 37 CFR 1.113. Official notice unsupported by documentary evidence should only be taken by the examiner where the facts asserted to be well-known, or to be common knowledge in the art are capable of instant and unquestionable demonstration as being well-known. As noted by the court in *In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970), the notice of facts beyond the record which may be taken by the examiner must be "capable of such instant and unquestionable demonstration as to defy dispute" (citing *In re Knapp Monarch Co.*, 296 F.2d 230, 132 USPQ 6 (CCPA 1961)).

As discussed above, none of the cited prior art shows a plurality of computers (not merely processors) that are arranged on a single, unitary substrate. Where this important aspect of Applicant's invention has not been shown in the prior art, it is error for the Examiner to conclude that asynchronous communication and asynchronous operation between computers located on a unitary substrate is "capable of such instant and unquestionable demonstration as to defy dispute." Therefore, should the Examiner wish to maintain the current rejections, the Examiner is requested to provide evidence on the record regarding asynchronous communication and asynchronous internal operation of multiple computers integrated on a unitary substrate pursuant to M.P.E.P. § 2144.03(C).

Claim 15:

Claim 15 is rejected under 35 U.S.C. §103(a) as being unpatentable over Fujii et al. and Pechanek1 in view of Common Art.

Applicants respectfully request reconsideration.

Claim 15 depends from Claim 14. Therefore, for the same reasons provided above with respect to Claim 14, because the combination of Fujii et al. and Pechanek1 fails to disclose all

the elements of the claim, the rejection of Claim 15 is improper. In addition, for the same reasons provided above with respect to Claims 5, 22, 29, 35, 43, 44, and 56, Applicant strongly objects to the Examiner taking official notice of elements of Claim 15 not disclosed by the cited references and respectfully requests that the Examiner provide evidence on the record if the Examiner wishes to maintain this rejection.

Claims 16, 31, and 33:

Claims 16, 31, and 33 are rejected under 35 U.S.C. §103(a) as being unpatentable over Fujii et al. and Pechanek1 in view of U.S. 6,173,380 (Pechanek et al., hereinafter "Pechanek2") and further in view of Common Art.

Applicants respectfully request reconsideration.

Claims 31 and 33 are canceled herein, thereby obviating the rejections of those claims.

Claim 16 depends from Claim 14 which recites that "each of the plurality of computers includes read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions." As stated above, because the combination of Fujii et al. and Pechanek1 fails to disclose the newly added elements of Claim 14, Claim 16 should now be distinguished over the cited prior art.

Pechanek2 similarly does not disclose the above recited limitation of amended Claim 14. The passage of Pechanek2 at column 8, lines 34-37 that is cited by the Examiner appears to refer to either SP data memory 121, data memory 123, or possibly VIM memory 109, which are shown in FIG. 3. However, as FIG. 3 shows, none of SP data memory 121, data memory 123, or VIM memory 109 are located within the processor elements 101, 151, 153, or 155 (note the dashed boxes defining the processor elements). Applicant also notes that item 125 in Pechanek2 is merely a data memory interface controller and does not appear to be active memory. Accordingly, processing elements 101, 151, 153, and 155 in Pechanek2 are merely processing elements and are not "computers." Therefore, Pechanek2 also does not disclose the above-recited limitation of Claim 14, from which Claim 16 depends.

Finally, for the same reasons provided above with respect to Claims 5, 22, 29, 35, 43, 44, and 56, Applicant strongly objects to the Examiner taking official notice of the elements of Claim 16 not disclosed by the cited references, and respectfully requests that the Examiner provide evidence on the record if the Examiner wishes to maintain this rejection.

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For the above reasons Applicant requests reconsideration and withdrawal of all the rejections under 35 U.S.C. § 103.

Other Amendments:

Claims 30 and 36 are amended to be consistent with the amendments made to Claim 1.

Claims 15 and 16 are amended to recite "an external flash memory" and "an external random access memory," respectively. Support for these amendments is provided at least at page 5, lines 13-22 and in FIG. 1.

No new matter is added.

For the foregoing reasons, Applicant believes that Claims 1-26, 29-30, 34-36, and 40-59 are in condition for allowance. Should the Examiner undertake any action other than allowance of Claims 1-26, 29-30, 34-36, and 40-59, or if the Examiner has any questions or suggestions for expediting the prosecution of this application, the Examiner is requested to contact Applicant's attorney at (269) 279-8820.

Respectfully submitted,

Date: 12/19/08

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Date: 12/19/08

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